IN THE CLAIMS:

1. (Withdrawn) A semiconductor device including a CMOS circuit having an NTFT and a PTFT, each of the NTFT and the PTFT including an active layer, an insulation film in contact with the active layer, and a wiring in contact with the insulation film, wherein

only the NTFT includes a side wall on a side of the wiring,

the active layer of the NTFT includes a channel forming region and at least three kinds of impurity regions each containing an element belonging to the group 15 at a different concentration,

the impurity region in contact with the channel forming region among the three kinds of impurity regions overlaps by way of the insulation film with the side wall,

the active layer of the PTFT includes a channel forming region and two kinds of impurity regions each containing an element belonging to the group 13 at an identical concentration, and

an element used for crystallization of the active layer of the NTFT and the active layer of the PTFT is present at a concentration not greater than 1×10^{20} atoms/cm^3 in one of the impurity region most remote from the channel forming region of the NTFT and in one of the impurity region most remote from the channel forming region of the PTFT.

2. (Withdrawn) A semiconductor device having a CMOS circuit having an NTFT and a PTFT, each of the NTFT and the PTFT including an active layer, an insulation film in contact with the active layer and a wiring in contact with the insulation film, wherein

only the NTFT includes a side wall on a side of the wiring,

the active layer of the NTFT includes a structure in which a channel forming region, a first impurity region, a second impurity region and a third impurity region are arranged in this order,

each of the first impurity region, the second impurity region and the third impurity region contains an element belonging to the group 15 at a different concentration,

the first impurity region overlaps by way of the insulation film with the side wall,

the active layer of the PTFT includes a structure in which a channel forming region, a fourth impurity region and a fifth impurity region are arranged in this order,

each of the fourth impurity region and the fifth impurity region contains an element belonging to the group 13 at an identical concentration and

an element used for the crystallization of the active layer is present at a concentration not greater than 1×10^{20} atoms/cm^3 in the third impurity region and the fifth impurity region.

3. (Withdrawn) A semiconductor device having a CMOS circuit having an NTFT and a PTFT each of the NTFT and the PTFT including an active layer, an insulation film in contact with the active layer and a wiring in contact with the insulation film, wherein

only the NTFT includes a side wall on a side of the wiring,

the active layer of the NTFT includes a channel forming region and at least three kinds of impurity regions each containing an element belonging to the group 15 at a different concentration,

the concentration of the element belonging to the group 15 is higher as the distance from the channel forming region is greater in at least three kinds of impurity regions,

the active layer of PTFT includes a channel forming region and two kinds of impurity regions containing an element belonging to the group 13 at an identical concentration, and

the active layer of PTFT includes a channel forming region and two kinds of impurity regions containing an element belonging to the group 13 at an identical concentration, and in which

an element used for the crystallization of the active layer is present at a concentration not greater than 1×10^{20} atoms/cm^3 in the impurity region most remote from the channel forming region of the NTFT and in the impurity region most remote from the channel forming region of the PTFT.

4. (Withdrawn) A semiconductor device including a CMOS circuit having an NTFT and a PTFT each of the NTFT and the PTFT including an active layer, an

insulation film in contact with the active layer and a wiring in contact with the insulation film, wherein

only the NTFT includes a side wall on a side of the wiring,

the active layer of the NTFT has a structure in which a channel forming region, a first impurity region, a second impurity region and a third impurity region are arranged in this order,

each of the first impurity region, the second impurity region and the third impurity region contains identical impurities at a different concentration,

the concentration of the impurities is higher in the order of the first impurity region, the second impurity region and the third impurity region,

the active layer of the PTFT has a structure in which a channel forming region, a fourth impurity region and a fifth impurity region are arranged in this order,

each of the fourth impurity region and the fifth impurity region contains an element belonging to the group 13 at an identical concentration, and

an element used for the crystallization of the active layer of the NTFT and the active layer of the PTFT is present at a concentration not greater than 1×10^{20} atoms/cm^3 in the third impurity region and the fifth impurity region.

5. (Withdrawn) A semiconductor device as claimed in any one of claims 1 to 4, wherein the active layer includes a single crystal semiconductor thin film.

6. (Withdrawn) A semiconductor, device as claimed in any one of claims 1 to 4, wherein the element used for crystallization is at least one selected from Ni, Ge, Co, Fe, Pd, Sn, Pb, Pt, Cu, Au and Si.

7. (Withdrawn) A semiconductor device as claimed in any one of claims 1 to 4, wherein at least a portion of the wiring is covered with a silicon nitride film.

8 (Withdrawn) A semiconductor device as claimed in any one of claims 1 to 4, wherein the side wall includes silicon.

9. (Withdrawn) A semiconductor device as claimed in claim 1 or 3, wherein the element belonging to the group 15 is present in one of the impurity regions of the

NTFT and in one of the impurity regions of the PTFT at a concentration identical. with each other, the element used for crystallization being present in said one of the impurity regions of the NTFT and in said one of the impurity regions of the PTFT.

10. (Withdrawn) A semiconductor. device as claimed in claim 2 or 4, wherein the element belonging to the group 15 is present in the third impurity region and in the fifth impurity region at a concentration identical with each other.

11. (Withdrawn) A semiconductor device as claimed in claim 2 or 4, wherein the element belonging to the group 15 is present in the third impurity region and in the fifth impurity region at a concentration identical with each other, and the concentration of the element belonging to the group 15 is lower than the concentration of the element belonging to the group 13 present in the fifth impurity region.

12. (Withdrawn) A semiconductor device as claimed in claim 2 or 4, wherein the concentration of the impurity contained in the first impurity region is $1 \times 10^{15} - 1 \times 10^{17}$ atoms/cm^3, and the concentration of the impurity contained in the second impurity region is $1 \times 10^{16} - 1 \times 10^{19}$ atoms/cm^3.

13. (Withdrawn) A semiconductor device as claimed in any one of claims 1 to 4, wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

14. (Withdrawn) A semiconductor device as claimed in any one of claims 1 to 4, wherein the semiconductor device is one selected from a video camera, a digital camera, a projector, a goggle type display, a car navigation device, a personal computer and a portable information terminal.

15.- 30. (Canceled)

31. (Withdrawn) A semiconductor device according to any one of claims 1 to 4 wherein the concentration of the element is not smaller than 1×10^{17} atoms/cm^3.

32. (Previously Presented) A semiconductor device comprising:

a semiconductor film formed on an insulating surface;

a channel forming region in the semiconductor film;

a gate insulating film formed on the semiconductor film;

a gate electrode formed over the channel forming region with the gate insulating film interposed therebetween;

a pair of side walls adjacent to side surfaces of the gate electrode;

an insulating film on the gate electrode and the pair of side walls;

a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the semiconductor film with the channel forming region extending therebetween wherein the pair of side walls only overlap the pair of first impurity regions; and

a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first concentration and formed in the semiconductor film adjacent to the pair of first impurity regions; and

a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the semiconductor film with the pair of second impurity regions extending between the channel forming region and the pair of third impurity regions.

33. (Previously presented) The semiconductor device according to claim 32 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

34. (Previously presented) The semiconductor device according to claim 32 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

35. (Previously presented) The semiconductor device according to claim 32 wherein the side walls comprise silicon.

36. (Previously presented) The semiconductor device according to claim 32 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

37. (Previously presented) The semiconductor device according to claim 32 wherein the semiconductor device is one selected from a video camera, a digital camera, a projector, a goggle type display, a car navigation device, a personal computer and a portable information terminal.

38. (Previously presented) A semiconductor device comprising:

a semiconductor film formed on an insulating surface;

a channel forming region in the semiconductor film;

a gate insulating film formed on the semiconductor film;

a gate electrode formed over the channel forming region with the gate insulating film interposed therebetween;

a pair of conductive side walls adjacent to side surfaces of the gate electrode;

an insulating film on the gate electrode and the pair of conductive side walls;

a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the semiconductor film with the channel forming region extending therebetween wherein the pair of side walls only overlap the pair of first impurity regions; and

a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first concentration and formed in the semiconductor film adjacent to the pair of first impurity regions; and

a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the semiconductor film with the pair of second impurity regions extending between the channel forming region and the pair of third impurity regions.

39. (Previously presented) The semiconductor device according to claim 38 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

40. (Previously presented) The semiconductor device according to claim 38 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

41. (Previously presented) The semiconductor device according to claim 38 wherein the side walls comprise silicon.

42. (Previously presented) The semiconductor device according to claim 38 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

43. (Previously presented) The semiconductor device according to claim 38 wherein the semiconductor device is one selected from a video camera, a digital camera, a projector, a goggle type display, a car navigation device, a personal computer and a portable information terminal.

44. (Previously presented) A semiconductor device comprising:

(a) a thin film transistor over a substrate, said thin film transistor comprising:

a semiconductor film formed on an insulating surface;

a channel forming region in the semiconductor film;

a gate insulating film formed on the semiconductor film;

a gate electrode formed over the channel forming region with the gate insulating film interposed therebetween;

a pair of side walls adjacent to side surfaces of the gate electrode;

an insulating film on the gate electrode and the pair of side walls;

a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the semiconductor film with the channel forming region extending therebetween wherein the pair of side walls only overlap the pair of first impurity regions; and

a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first concentration and formed in the semiconductor film adjacent to the pair of first impurity regions; and

a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the semiconductor film with the pair of second impurity regions extending between the channel forming region and the pair of third impurity regions;

(b) an interlayer insulating film formed over the thin film transistor; and

(c) a pixel electrode formed over the interlayer insulating film and electrically connected to one of the third impurity regions.

45. (Previously presented) The semiconductor device according to claim 44 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

46. (Previously presented) The semiconductor device according to claim 44 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

47. (Previously presented) The semiconductor device according to claim 44 wherein the side walls comprise silicon.

48. (Previously presented) The semiconductor device according to claim 44 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

49. (Previously presented) The semiconductor device according to claim 44 wherein the semiconductor device is one selected from a video camera, a digital camera, a projector, a goggle type display, a car navigation device, a personal computer and a portable information terminal.

50. (Previously presented) A semiconductor device comprising:

(a) a thin film transistor formed over a substrate, said thin film transistor comprising:

a semiconductor film formed on an insulating surface;

a channel forming region in the semiconductor film;

a gate insulating film formed on the semiconductor film;

a gate electrode formed over the channel forming region with the gate insulating film interposed therebetween;

a pair of conductive side walls adjacent to side surfaces of the gate electrode;

an insulating film on the gate electrode and the pair of conductive side walls;

a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the semiconductor film with the channel forming region extending therebetween wherein the pair of side walls only overlap the pair of first impurity regions; and

a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first concentration and formed in the semiconductor film adjacent to the pair of first impurity regions; and

a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the semiconductor film with the pair of second impurity regions extending between the channel forming region and the pair of third impurity regions;

(b) an interlayer insulating film formed over the thin film transistor; and

(c) a pixel electrode formed over the interlayer insulating film and electrically connected to one of the third impurity regions.

51. (Previously presented) The semiconductor device according to claim 50 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

52. (Previously presented) The semiconductor device according to claim 50 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

53. (Previously presented) The semiconductor device according to claim 50 wherein the side walls comprise silicon.

54. (Previously presented) The semiconductor device according to claim 50 wherein the semiconductor device is one selected from a liquid crystal display device, and EL display device and an image sensor.

55. (Previously presented) The semiconductor device according to claim 50 wherein the semiconductor device is one selected from a video camera, a digital camera, a projector, a goggle type display, a car navigation device, a personal computer and a portable information terminal.

56. – 59. (Canceled)

60. (New) A semiconductor device comprising:

a semiconductor film formed on an insulating surface;

a channel forming region in the semiconductor film;

a gate insulating film formed on the semiconductor film;

a gate electrode formed over the channel forming region with the gate insulating film interposed therebetween;

a second insulating film in contact with an upper surface and side surfaces of the gate electrode;

a pair of side walls adjacent to the side surfaces of the gate electrode with the second insulating film interposed therebetween;

a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the semiconductor film with the channel forming region extending therebetween wherein the pair of side walls only overlap the pair of first impurity regions; and

a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first concentration and formed in the semiconductor film adjacent to the pair of first impurity regions; and

a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the semiconductor film with the pair of second impurity regions extending between the channel forming region and the pair of third impurity regions.

61. (New) The semiconductor device according to claim 60 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

62. (New) The semiconductor device according to claim 60 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

63. (New) The semiconductor device according to claim 60 wherein the side walls comprise silicon.

64. (New) The semiconductor device according to claim 60 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

65. (New) The semiconductor device according to claim 60 wherein the semiconductor device is one selected from a video camera, a digital camera, a projector, a goggle type display, a car navigation device, a personal computer and a portable information terminal.

66. (New) A semiconductor device comprising:

(a) a thin film transistor over a substrate, said thin film transistor comprising:

a semiconductor film formed on an insulating surface;

a channel forming region in the semiconductor film;

a gate insulating film formed on the semiconductor film;

a gate electrode formed over the channel forming region with the gate insulating film interposed therebetween;

a second insulating film in contact with an upper surface and side surfaces of the gate electrode;

a pair of side walls adjacent to the side surfaces of the gate electrode with the second insulating film interposed therebetween;

a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the semiconductor film with the channel forming region

extending therebetween wherein the pair of side walls only overlap the pair of first impurity regions; and

a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first concentration and formed in the semiconductor film adjacent to the pair of first impurity regions; and

a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the semiconductor film with the pair of second impurity regions extending between the channel forming region and the pair of third impurity regions;

(b) an interlayer insulating film formed over the thin film transistor; and

(c) a pixel electrode formed over the interlayer insulating film and electrically connected to one of the third impurity regions.

67. (New) The semiconductor device according to claim 66 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

68. (New) The semiconductor device according to claim 66 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

69. (New) The semiconductor device according to claim 66 wherein the side walls comprise silicon.

70. (New) The semiconductor device according to claim 66 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

71. (New) The semiconductor device according to claim 66 wherein the semiconductor device is one selected from a video camera, a digital camera, a projector, a goggle type display, a car navigation device, a personal computer and a portable information terminal.

72. (New) A semiconductor device comprising a CMOS circuit comprising:

an NTFT having:

a first semiconductor film formed on an insulating surface;

a first channel forming region in the first semiconductor film;

a first gate insulating film formed on the first semiconductor film;

a first gate electrode formed over the first channel forming region with the first gate insulating film interposed therebetween;

a pair of side walls adjacent to side surfaces of the first gate electrode;

a second insulating film on the first gate electrode and the pair of side walls; and

a PTFT having:

a second semiconductor film formed on an insulating surface;

a second channel forming region in the second semiconductor film;

a third gate insulating film formed on the second semiconductor film;

a second gate electrode formed over the second channel forming region with the third gate insulating film interposed therebetween;

wherein a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the first semiconductor film with the first channel forming region extending therebetween wherein the pair of side walls only overlap the pair of first impurity regions;

wherein a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first concentration and formed in the first semiconductor film adjacent to the pair of first impurity regions; and

wherein a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the first semiconductor film with the pair of second impurity regions extending between the first channel forming region and the pair of third impurity regions.

73. (New) The semiconductor device according to claim 72 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

74. (New) The semiconductor device according to claim 72 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

75. (New) The semiconductor device according to claim 72 wherein the side walls comprise silicon.

76. (New) The semiconductor device according to claim 72 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

77. (New) The semiconductor device according to claim 72 wherein the semiconductor device is one selected from a video camera, a digital camera, a projector, a goggle type display, a car navigation device, a personal computer and a portable information terminal.

78. (New) A semiconductor device comprising a CMOS circuit comprising:

an NTFT having:

a first semiconductor film formed on an insulating surface;

a first channel forming region in the first semiconductor film;

a first gate insulating film formed on the first semiconductor film;

a first gate electrode formed over the first channel forming region with the first gate insulating film interposed therebetween;

a second insulating film in contact with an upper surface and side surfaces of the first gate electrode;

a pair of side walls adjacent to the side surfaces of the first gate electrode with the second insulating film interposed therebetween; and

a PTFT having:

a second semiconductor film formed on an insulating surface;

a second channel forming region in the second semiconductor film;

a third gate insulating film formed on the second semiconductor film;

a second gate electrode formed over the second channel forming region with the third gate insulating film interposed therebetween;

wherein a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the first semiconductor film with the first channel forming region extending therebetween wherein the pair of side walls only overlap the pair of first impurity regions;

wherein a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first concentration and formed in the first semiconductor film adjacent to the pair of first impurity regions; and

wherein a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the first semiconductor film with the pair of second impurity regions extending between the first channel forming region and the pair of third impurity regions.

79. (New) The semiconductor device according to claim 78 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

80. (New) The semiconductor device according to claim 78 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

81. (New) The semiconductor device according to claim 78 wherein the side walls comprise silicon.

82. (New) The semiconductor device according to claim 78 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

83. (New) The semiconductor device according to claim 78 wherein the semiconductor device is one selected from a video camera, a digital camera, a projector, a goggle type display, a car navigation device, a personal computer and a portable information terminal.